Modeling MOSFETs for fault-managed power systems: a transient analysis based on capacitance dynamics

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***Abstract*—The nonlinear, dynamic change in junction capacitance of MOSFETs during switching is crucial in modeling and analyzing the transients in Switched-Mode Power Supplies. In this paper, these dynamics are addressed and an improved MOSFET model is developed for applications in fault-managed power systems. The momentary change in MOSFET parasitics is modeled based on generic equations to analyze the switching performance in different load conditions. The developed model has shown a certain degree of accuracy required to define safe operating conditions for precise fault detection in fault-managed power systems. The change in gate capacitance is shown and used in updating the MOSFET model. The proposed model is simulated in Simscape and the accuracy of the model is validated using experimental data from test circuits with various load combinations.**

***Index Terms*—Fault-managed Power Systems, MOSFET switching, Dynamic Junction Capacitance, Class 4 Power**

I. Introduction

Fault management in power systems has been a prime concern for different types of power delivery protocols. Over the years, different schemes have been proposed for managing faults in various power system applications [1]- [4]. However, most of the approaches have been made with the conventional AC/DC power system models. The recent advances in intelligent power delivery methods, especially fault-managed power systems (FMPS) have been drawing more interest than ever. The promise of safer electricity has made its way into the U.S. National Electric Code 2023 as a new class of power delivery method. FMPS are expected to increase the safety, efficiency and simplicity of power systems in data centers, industrial environments, EV charging and commercial buildings. The FMPS which are referred to as 'Class 4 Power Systems' in the National Electric Code (NEC), Article 726, are not power limited with respect to risk of electric shock and fire hazards. These systems are able to transfer more power than the NEC Article 725 Class 2 systems while mitigating more risk than the NEC Chapter 3 systems. For example, whereas a Class 2 PoE system is limited to 100W, a Class 4 power system could provide 10x that power or more while still providing protection against electric shock and fire hazards within an acceptable level of risk. Ensuring the safety of these power systems, the need for modeling the switching transients more accurately to predict and analyse the system behavior has become essential to avoid errors in detecting faults. For smart fault detection, safety features are now getting embedded in the power delivery schemes, and addressing the component-level responses of the power systems accurately has been crucial from a designing and modeling perspective. In this effort, we have modeled and analyzed the switching performance of the MOSFETs in pulsed DC systems. Switching performance is one of the major parameters considered while designing power converters.

MOSFETs are popular choices for designing and developing Switch Mode Power Supplies for their low-loss and highly efficient switching characteristics and plays one of the most vital roles in converters. While the on-resistance is considered one of the primary parameters in selecting MOSFETs for different applications, other parameters like capacitance, parasitic inductance, gate charge are also of high importance in design, modeling and predictive analysis of power converters at different load conditions. Various methods have been proposed for developing the nonlinear parasitic capacitance to model switching transients in Switched-Mode Power Supplies (SMPS) in [5] and [6]. A more detailed discussion on estimating the dynamic parasitic capacitance in transient analysis in [7] - [9] is the basis of the modeling approach for MOSFETs used in FMPS. In this article, an improved MOSFET model is introduced that incorporates the nonlinear, dynamic parasitic effects during switching transients. In section II, the mathematical model for switching transients and their impact on the dynamics of the impedance profile of the MOSFET is developed. The following section discusses how the test setup was designed and shows the captured wave shapes from the experiments. The developed model is validated using the comparison graphs of test data and simulated data using Simscape and discusses the findings from the analysis. Finally, the key results from the study and their impact on the applications in fault managed power systems are noted in section V.

The major development the proposed model has over the previous models is it incorporates the dynamic change in capacitance during switching and replicates the total impedance of the system instantaneously so the transients can be simulated more accurately. The inclusion of the proposed MOSFET model into fault managed power system circuits enables us to address the possible swift changes in voltage and current levels that prevents the circuit from tripping in the event of a false alarm due to the switching transients.

II. Model Development

MOSFET turn on or turn off is not an event, but rather it is a process. During the process, there are phases where the charges are injected into the gate (during turn on) or removed from the gate (during turn off). In an isolated circuit, the process can be derived mathematically using the junction capacitance. The MOSFET gate comprises of two input capacitors (C_{gd} and C_{gs}) and an internal gate resistor R_g. When the gate is supplied with a step voltage V_{GS}, the output response can be obtained. MOSFET turn on and turn off behavior can be described in the timing diagrams in Fig. 1 and Fig. 2. Throughout this paper, the uppercase subscripts refer to the rated or applied quantities, while time varying or measured quantities will be denoted by lower case subscripts. The effective input capacitance can be defined as $C_{iss} = C_{gs} + C_{gd}$. It is important to note that these two nonlinear capacitors are not physically connected in parallel and carry different voltages. The total gate resistance R_G is the combination of the internal gate resistor R_g and external gate resistor R_{gext}. The simplified form of analytical equations, Eq. (1) - (6) developed by Baliga [9], is used to define each phase of the switching transients in time segments.

$$t_1 = R_G * C_{iss} * ln(\frac{1}{1 - \frac{V_{TH}}{V_{GS}}}) \quad (1)$$

$$t_2 = R_G * C_{iss} * ln(\frac{1}{1 - \frac{V_{gp}}{V_{GS}}}) \quad (2)$$

$$t_3 = R_G * C_{gd} * \frac{V_{DS}}{V_{GS} - V_{gp}} \quad (3)$$

Here, V_{DS}, V_{gp} and V_{TH} are the voltage across drain to source, plateau voltage and gate threshold voltage, respectively. From Fig. 1, time segments t_1 and t_2 can be calculated accurately but it is tough to calculate t_3 due to the quick change in V_{DS} as well as C_{gd}. The gate charge specified in the data sheet is useful for calculating the time.

$$t_4 = R_G * C_{iss} * ln(\frac{V_{GS}}{V_{gp}}) \quad (4)$$

$$t_5 = R_G * C_{gd} * ln(\frac{V_{DS}}{V_{gp}}) \quad (5)$$

$$t_6 = R_G * C_{iss} * ln(\frac{V_{gp}}{V_{TH}}) \quad (6)$$

For the turn off, similar analysis applies for the calculation of the time segments depicted in Fig. 2. While t_4 and t_6 are straightforward, the plateau voltage duration t_5 is a little complicated due to the change in C_{gd}. Instead of using any absolute value for the capacitance, the change in C_{gd} and in turn the effective input capacitance C_{iss} is calculated from the test measurements and later validated with the simulation results.

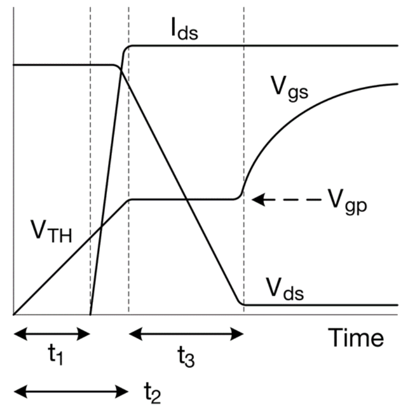

Fig. 1. Transient response of MOSFET during turn on

The gate charge waveform from Fig. 3 shows the charge Q_{GS} from initialization to the start of the Miller plateau voltage V_{gp}, where the charge Q_{gd} corresponds to the charge accumulated during the entire plateau period and Q_G is the total charge from the origin to the actual driving voltage V_{GS}.

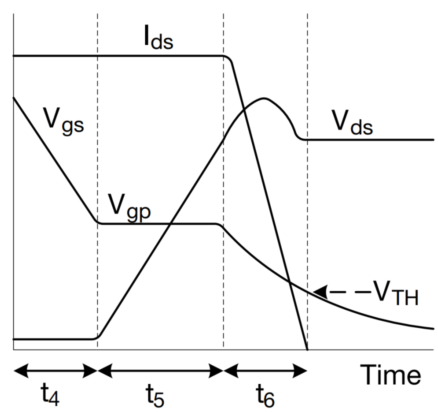

Fig. 2. Transient response of MOSFET during turn off

For a near-zero slope in plateau voltage, all the driving current during t_5 flows into C_{gd} and the charge Q_{gd} is injected into the MOSFET gate. This happens when there is a rapid increase in the $C_{gd} * V_{gd}$ product. After the plateu region, C_{gd} attains a fixed value again and the bulk current flows through C_{gs}.

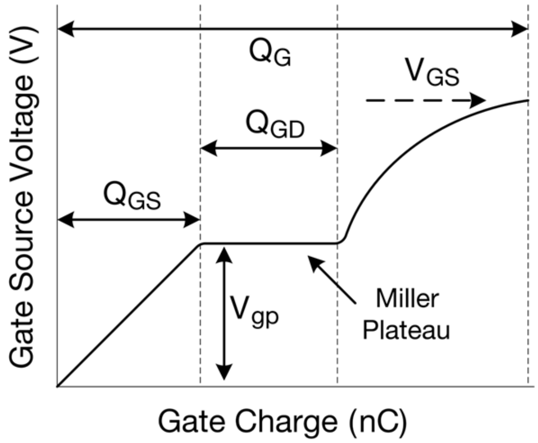

Fig. 3. Gate Charge breakdown in MOSFET

Combining the gate charge and capacitance to calculate the time segments t_3 and t_5 modifies the Eq. (3) and Eq. (5) into the following:

$$t_3 = R_G * \frac{Q_{GD(D)}}{V_{DS(D)}} * \frac{V_{DS}}{V_{GS} - V_{gp}} \quad (7)$$

$$t_5 = R_G * \frac{Q_{GD(D)}}{V_{DS(D)}} * \frac{V_{DS}}{V_{gp}} \quad (8)$$

Here, $Q_{GD(D)}$ and $V_{DS(D)}$ refers to the data sheet values of the MOSFET. The switching transients are calculated using the model described here and compared with the test data from the experimental setup discussed in the next section.

III. Test Setup and Data Acquisition

A simple MOSFET test circuit board was used for the test setup. The MOSFET was connected to the load. The simple circuit model is illustrated in Fig. 4. The MOSFET was tested with a pure resistive load ($R = 50\Omega$) as well as an inductive load ($R = 50\Omega$ and $L = 10\mu H$). The source voltage ranged from 5V to 100V. As for using an external gate resistor, two different resistor values ($Rg_{ext} = 680\Omega$ and 270Ω) have been used to observe the change in switching speed.

Fig. 5 shows the test circuit board. Most of the components on the board were not connected to the test setup to keep the circuit as simple as possible. For capture and measurement, V_{DS}, V_{GS} and V_{GD} were probed along with the current through the MOSFET I_{ds}.

Fig. 6 shows the oscilloscope capture of the test data that has been used to compare and calculate the MOSFET parameters. The change in drain-to-source voltage, V_{DS}, and the time duration of Miller Plateau t_5 during turn off have been measured and used to calculate the capacitance C_{gd}. The tests have been repeated for different configurations and different source voltages. The gate and source on the circuit board were clamped by using a large resistor $R_{gs} = 1\text{M}$.

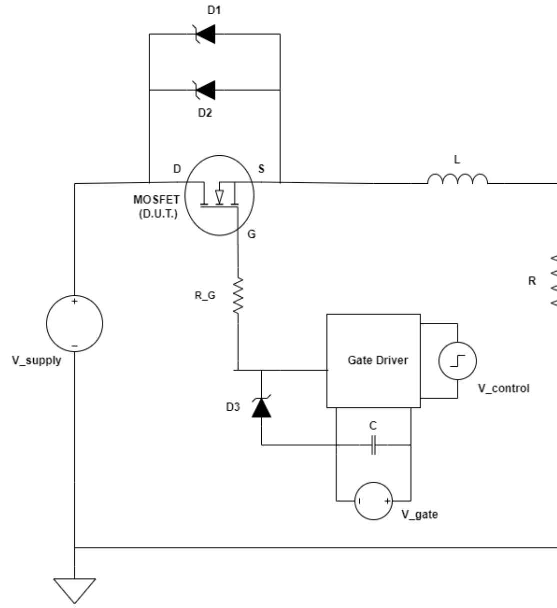

Fig. 4. MOSFET test circuit

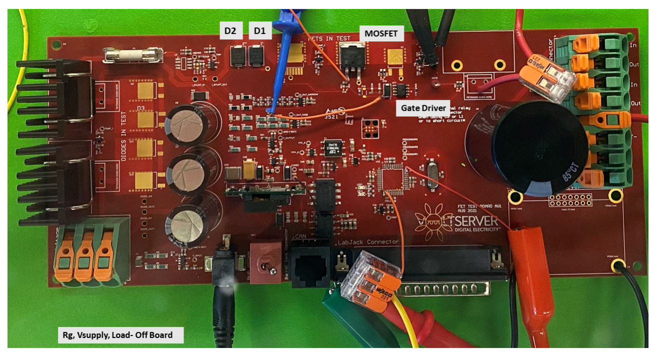

Fig. 5. Experimental test setup

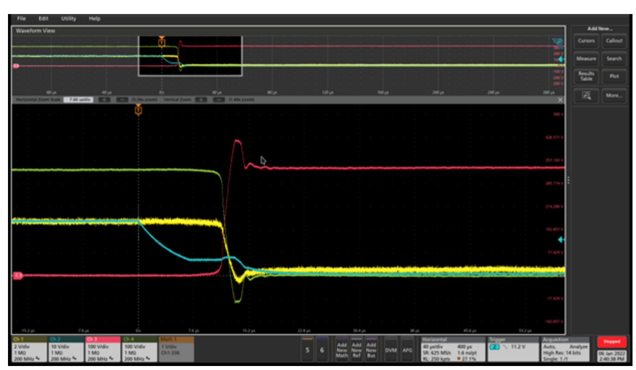

Fig. 6. Oscilloscope capture from test circuit

IV. Comparative analysis for validation

In order to validate the mathematical model, an improved MOSFET model is developed in MATLAB Simscape using the empirical data from the tests. The exact circuit has been modeled and simulated. Plugging in the time duration, gate charge, plateau voltage and drain-to-source voltage data into the equations [1-8] described in section II, the capacitances C_{gd}, C_{iss} are calculated. The change in C_{gd} depending on the V_{DS} for different test conditions is shown in Fig. 7.

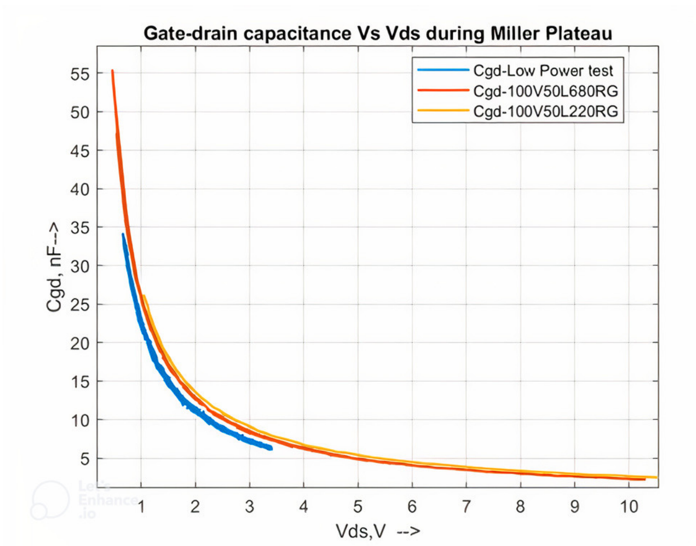

Fig. 7. Capacitance sweep during Miller plateau in turn off transient

Here, the low power test labeled in Fig. 7 refers to a 5V source supply in the circuit illustrated in Fig. 4. The inclusion of the capacitance sweep in tabulated capacitance of the Simscape MOSFET model replicated the dynamic response of the real-world MOSFET behavior with a reasonable accuracy.

Fig. 8 shows the comparison graph for the V_{GS} curve from the test data and simulated results. The only difference in the comparison is the dV/dt shoot-through condition [10] at the very edge of the Miller plateau . The accuracy in the modeling is of prime importance since for fault-manged power systems, it is essential to address all the corner cases in transient response during switching in order to define safe operating conditions.

V. Conclusion

This work emphasized on developing an accurate MOSFET model used for different SMPS circuits for fault-management applications. The generic equations for transient response of the MOSFETs were used to calculate the MOSFET parameters such as dynamic junction capacitance. The experimental test set up allowed to observe and inspect the response of the MOSFET under different test conditions. The empirical data and mathematical model were used to determine the parameters for MOSFET properties, these properties were used in the simulation model and finally the simulated data were compared with test data from an identical circuit configuration

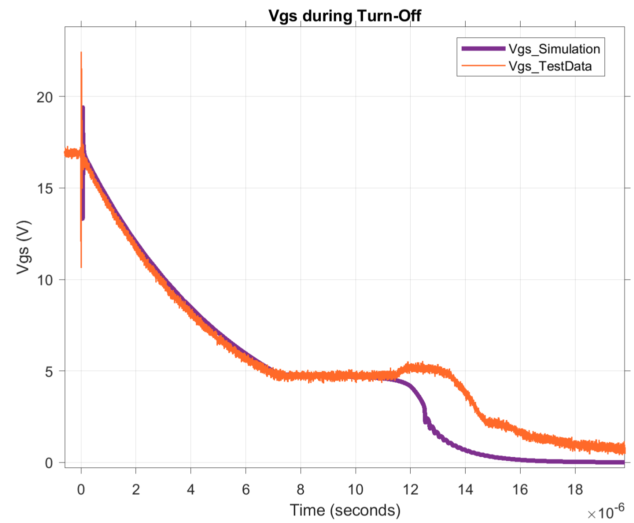

Fig. 8. Comparison graph for V_{GS} from test and simulation data

for the model validation. The major takeaways from this work are understanding how the dynamics of MOSFET parameters during transitions can help predict the system response more accurately and in turn improve the system design greatly while ensuring safety of the equipment such as power converter circuits and various loads depending on the application. Moreover, the findings of the study can aid to improve design of different applications like renewable energy integration to the grid, electric vehicle charging systems, battery electronics etc. In the future, the study and experiments can be extended to use the improved MOSFET models in different power delivery and other industry application, especially for fault-managed power systems.

VI. Acknowledgement

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